UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,618	09/22/2003	Hongwei Wang	1875.5060000	6566

26111 7590 06/17/2004

STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
NGUYEN, JOHN B	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/665,618	WANG, HONGWEI	
	Examiner	Art Unit	
	John B Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,8 and 12-17* is/are rejected.

7)☒ Claim(s) *3,6,9-11 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 5, 7, 8, 12 -17 are rejected under 35 U.S.C. 102(b) as being anticipated by Dedic (US Patent No. 6,100,830).

3. Regarding to claim 1, Fig. 2-11, Dedic disclose a system, comprising a digital section (12, 14), including a first driving device (DRIVER 1) having a switch (SW1) and a logic gate (DRIVER 1), the first driving device configured to receive a first digital signal (IN1) and generate a first drive signal (output from 12), and a second driving device (DRIVER 2) having a switch (SW2) and a logic gate (DRIVER 2), the second driving device configured to receive a second digital signal (IN2) and generate a second drive signal (output from 14), and an analog section (S1, S2) configured to receive the first and second drive signals (output from 12 and 14) and generate first and second respective analog signals (OUT1 and OUT2), wherein rise and fall times of the first and second drive signals are substantially equal (column 13, lines 7-15 and lines 54-59).

4. Regarding to claim 2, the system of claim 1, wherein the logic gates in the first and second driving devices are NOR gates (Fig.4, elements 12 and 14).

5. Regarding to claim 4, the system of claim 2, wherein the analog device (Fig. 4, S1, S2) comprises: a first p-type transistor device (column 8, line 32-34) receiving the first drive signal (receive output from 12) to generate the first analog signal (OUT1); and a second p-type transistor (column 8, line 32-34) receiving the second drive signal (receive output from 14) to generate the second analog signal (OUT2).

6. Regarding to claim 5, the system of claim 1, wherein the logic gates in the first and second driving devices are NAND gates (Fig. 6, elements 12, 14).

7. Regarding to claim 7, the system of claim 5, wherein the analog device (Fig 6, S1, S2) comprises: a first n-type transistor device (column 9, line 18-20) receiving the first drive signal (receive output from 12) to generate the first analog signal (OUT1); and a second n-type transistor device (column 9, line 18-20) receiving the second drive signal (receive output from 14) to generate the second analog signal (OUT2).

8. Regarding to claim 8, the system of claim 1, wherein the digital section (12, 14) further comprises: an acceleration system (Fig. 11, elements RC11, RC 12) coupled to the first and second driving devices (12, 14) and configured to accelerate the rise and fall times of the first and second drive signals (column 13, lines 7-19).

9. Regarding to claim 12, a system (fig. 2 -11) comprising: a digital section (12,14) configured to receive digital signals (IN1, IN2) including a means for generating first and second drive signals (output from 12, output from 14) having substantially equal rise and fall times (column 13, lines 7-15, lines 54-59); and an analog section (S1, S2)

configured to receive the first and second drive signals (receive output from 12, and receive output from 14) and generate first and second analog signals (OUT1, OUT2).

10. Regarding to claim 13, the system of claim 12, wherein the means for generating comprises first and second logic devices (DRIVER1, DRIVER2).

11. Regarding to claim 14, the system of claim 13, wherein the first and second logic devices are NOR gates (fig. 4, elements 12 and 14).

12. Regarding to claim 15, the system of claim 13, wherein the first and second logic devices are NAND gates (fig. 6, elements 12, 14).

13. Regarding to claim 16, the system of claim 12, wherein the digital section further comprises a means for accelerating the rise and fall times of the first and second drive signals (fig. 11, elements RC11 and RC12).

14. Regarding to claim 17, the system of claim 16, wherein the means for accelerating comprises first and second inverters (column 12, line 66-67; column 13, line 1-2).

Allowable Subject Matter

15. Claims 3, 6, 9-11 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. (See enclosed Form PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B Nguyen whose telephone number (571) 272-1808. The examiner can normally be reached on 8AM-4: 30 PM M-F.

John B. Nguyen
June 8, 2004